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06ES33

Third Semester B.E. Degree Examination, Dec. 07 / Jan. 08
Logic design

Time : 3 hrs. Max. Marks:100

Note : *1. Answer any FIVE full questions.*
2. Assume missing data if any suitably.

1 a. Two motors M_2 and M_1 are controlled by three sensors S_3, S_2 and S_1. One motor M_2 is to run any time all three sensors are on. The other motor is to run whenever sensors S_2 or S_1 but not both are on and S_3 is off. For all sensor combinations where M_1 is on, M_2 is to be off except when all the three sensors are off and then both motors must remain off. Construct the truth table and write the Boolean output equation. **(06 Marks)**

b. Simplify using Karnaugh map. Write the Boolean equation and realize using NAND gates. $D = f(w,x,y,z) = \Sigma(0,2,4,6,8) + \Sigma d(10,11,12,13,14,15)$. **(06 Marks)**

c. Simplify $P = f(a,b,c,) = \Sigma(0,1,4,5,7)$ using two variable Karnaugh map. Write the Boolean equation and realize using logic gates. **(08 Marks)**

2 a. Simplify using Karnaugh map $L = f(a,b,c,d) = \pi(2,3,4,6,7,10,11,12)$ **(06 Marks)**

b. Simplify using Quine Mc Cluskey tabulation algorithm-
$V = f(a,b,c,d) = \Sigma(2,3,4,5,13,15) + \Sigma d(8,9,10,11)$ **(14 Marks)**

3 a. Design a combinational circuit that will multiply two two-bit binary values. **(08 Marks)**

b. Design a 4 to 16 decoder using two 3 to 8 decoder (74LS138). **(06 Marks)**

c. Design a keypad interface to a digital system using ten line BCD encoder (74LS147). **(06 Marks)**

4 a. Design a binary full subtractor using minimum number of gates. **(06 Marks)**

b. Explain the terms
i) Ripple – carry propagation
ii) Propagation delay
iii) Look- ahead carry
iv) Iterative design. **(04 Marks)**

c. Realize $F = f(x,y,z,) = \Sigma(1,2,4,5,7)$ using 8 – to – 1 multiplexer (74LS151). **(04 Marks)**

d. Design a two bit binary magnitude comparator. **(06 Marks)**

5 a. Explain with timing diagram the working of a S. R latch as a switch debouncer. **(06 Marks)**

b. Explain the working of a Master – slave JK Flip-Flop with functional table and timing diagram. Show how race around condition of master-slave SR Flip-Flop is over come. **(08 Marks)**

c. What is the significance of edge triggering? Explain the working of edge triggered D-flip-flop and T-flip-flop with their functional table. **(06 Marks)**

6 a. Obtain the characteristic equation for a SR flip-flop **(04 Marks)**

b. With a neat circuit diagram, explain the working of a universal shift register. **(08 Marks)**

c. Design a synchronous Mod-6 counter using clocked J K flip-flop. **(08 Marks)**

7 a. Explain mealy and Moore sequential circuit models. (04 Marks)

b. For the state machine M_1 shown in Fig. Q 7(b), obtain
   i) State table
   ii) Transition table
   iii) Exaltation table for T flip-flop
   iv) Logic circuit for T exaltation realization.

(16 Marks)

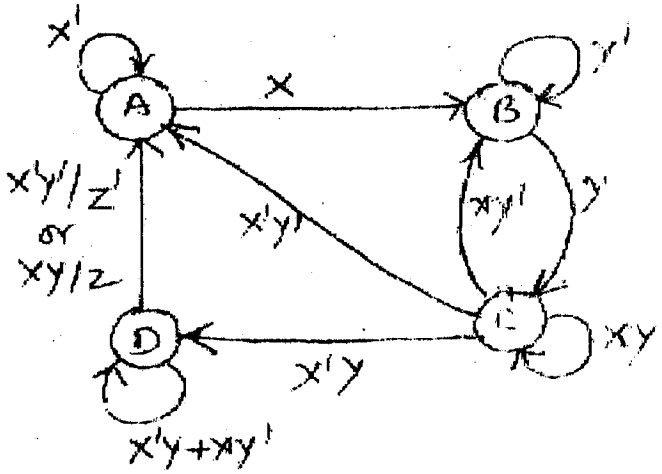

Fig. Q 7(b)

8 a. Construct a mealy state diagram that will detect a serial sequence of 10110. When the input pattern has bee detected, cause an output Z to be asserted high. (08 Marks)

b. Design a cyclic modulo-8 synchronous counter using J–K flip-flop that will count the number of occurrences of an input; that is, the number of times it is a 1. The input variable X must be coincident with the clock to be counted. The counter is to count in binary. (12 Marks)

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06ES33

Third Semester B.E. Degree Examination, June / July 08
Logic Design

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE questions, choosing atleast two from each part.***

PART - A

1 a. Simplify the following expression using Karnaugh Map. Implement the simplified circuit using the gates as indicated.

i) $f(ABCD) = \Sigma m(2,3,4,5,13,15) + \Sigma\alpha(8,9,10,11)$ use only NAND gates

ii) $f(ABCD) = \pi(2,3,4,6,7,10,11,12)$ use only NOR gates

to implement these circuits. **(12 Marks)**

b. Fig shows a BCD counter that produces a 4 –bit output representing the BCD code for the number of pulses that have been applied to the counter input. For example, after four pulses have occurred, the counter outputs are $(ABCD) = (0100)_2 = (04)_{10}$. The counter resets to 0000 on the tenth pulse and starts counting over again. Design the logic circuit that produces a HIGH output. Whenever the count is 2, 3 or 9. Use K – mapping and take advantages of "don't care" conditions. Implement the logic circuit using NAND gates.

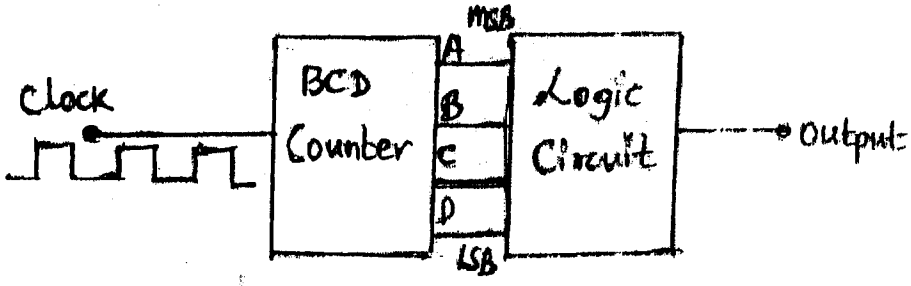

Fig. Q 1(b) **(08 Marks)**

2 a. Simplify the logic function given below, using Quine–McCluskey minimization technique. $Y(ABCD) = \Sigma m(0,1,3,7,8,9,11,15)$. Realize the simplified expression using universal gates. **(12 Marks)**

b. Simplify the logic function given below using variable – entered mapping (VEM) technique. $Y(ABCD) = \Sigma m(1,3,4,5,8,9,10,15) + \Sigma d(2,7,11,12,13)$. **(08 Marks)**

3 a. Realize the following Boolean function $f(ABCD) = \Sigma(0,1,3,5,7)$

Using – i) 8 : 1 MUX(74151) ii) 4 : 1 MIX(74153). **(08 Marks)**

b. Design a combinational logic circuit that will convert a straight BCD digit to an Excess – 3 BCD digits.

i) Construct the truth table

ii) Simplify each output function using Karnaugh Map and write the reduced equations.

iii) Draw the resulting logic diagram. **(12 Marks)**

4 a. Design a 4 – bit BCD adder circuit using 7483 IC chip, with self correcting circuit. i.e., a provision has to be made in the circuit, in case if the sum of the BCD number exceeds 9. **(12 Marks)**

b. Design a combinational circuit that accepts two unsigned 2 – bit binary number and provides 3 outputs.

Inputs : word $A = A_1A_0$, word $B = B_1B_0$.

Output : A = B, A>B, A<B. **(08 Marks)**

PART - B

5 a. Derive the characteristics equations of the following flip flops.
i) SR flip flops ii) JK flip flop. (10 Marks)

b. Explain clearly the operation of an asynchronous inputs in a flip flops with suitable example. (06 Marks)

c. An edge triggered 'D' flip flop is connected as shown in the Fig. Q 5(b). Assume that Q = 0 initially and sketch the wave form and determine its frequency of the signal at 'Q' output.

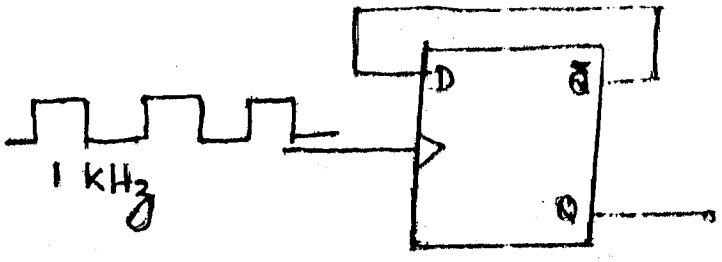

Fig. Q 5(C) (04 Marks)

6 a. With the help of a suitable example, explain the following operations in a shift register.
i) SISO ii) PISO iii) Twisted ring counter (10 Marks)

b. Design a ripple counter to count the following sequence, 1111 1110, 1101, 1100, 1011, 1111, 1110, 1101, 1100, 1011, etc. Suggest a suitable circuit using 7490 and other gates to obtain the desired result. (10 Marks)

7 a. With a suitable example, explain the Mealy and Moore Model of a sequential circuit. (10 Marks)

b. Construct the state table for the following state diagram.

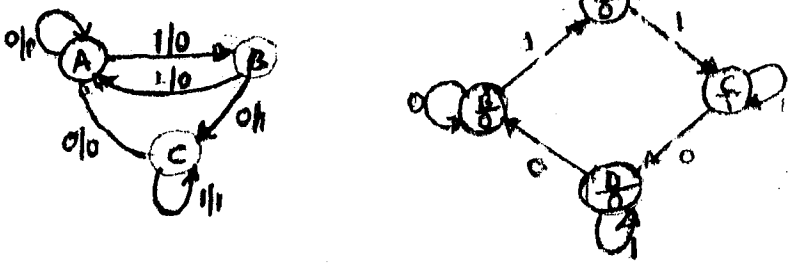

Fig. Q 7(c) (10 Marks)

8 a. Design a clocked sequential circuit that operates according to the state diagram shown. Implement the circuit using D – flip flop.

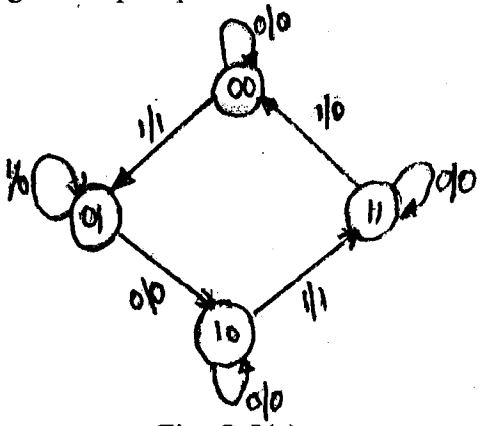

Fig. Q 8(a) (12 Marks)

b. Design a counter using JK – flip flops whose counting sequence is 000, 001, 100, 110, 111,101, 000 etc. by obtaining its minimal sum equations. (08 Marks)

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06ES33

Third Semester B.E. Degree Examination, Dec.08/Jan.09
Logic Design

Time: 3 hrs. Max. Marks:100

Note:1. ***Answer any FIVE full questions, choosing at least two questions from each part A & B.***
2. ***Missing data be suitably assumed.***

Part A

1 a. Convert the given boolean function $f(x,y,z)=[x+\bar{x}\bar{z}(y+\bar{z})]$ into maxterm canonical formula and hence highlight the importance of canonical formula. **(05 Marks)**

b. Distinguish the prime implicants and essential prime implicants. Determine the same of the function $f(w,x,y,z)=\sum m(0,1,4,5,9,11,13,15)$ using K-map and hence the minimal sum expression. **(05 Marks)**

c. Design a combinational logic circuit, which converts BCD code into Excess-3 code and draw the circuit diagram. **(10 Marks)**

2 a. Using Quine-Mcluskey method and prime implicant reduction table, obtain the minimal sum expression for the Boolean function $f(w,x,y,z)=\sum m(1,4,6,7,8,9,10,11,15)$. **(12 Marks)**

b. Obtain the minimal product of the following Boolean functions using VEM technique:
$f(w,x,y,z)=\sum m(1,5,7,10,11)+dc(2,3,6,13)$ **(08 Marks)**

3 a. Realize the following functions expressed in maxterm canonical form in two possible ways using 3–8 line and decoder:
$f_1(x_2,x_1,x_0)=\pi M(1,2,6,7)$
$f_2(x_2,x_1,x_0)=\pi M(1,3,6,7)$ **(10 Marks)**

b. What are the problems associated with the basic encoder? Explain, how can these problems be overcome by priority encoder, considering 8 input lines. **(10 Marks)**

4 a. Implement the function $f(w,x,y,z)=\sum m(0,1,5,6,7,9,10,15)$ using a 4 : 1 MUX with w, x as select lines: **(08 Marks)**

b. The 1-bit comparator had 3 outputs corresponding to x > y, x = y and x < y. It is possible to code these three outputs using two bits S_1S_0 such as S_1, S_0 = 00, 10, 01 for x = y, x > y and x < y respectively. This implies that only two-output lines occur from each 1–bit comparator. However at the output of the last 1–bit comparator, an additional network must be designed to convert the end results back to three outputs. Design such a 1–bit comparator as well as the output converter network. **(12 Marks)**

Part B

5 a. What is a Flip Flop? Discuss the working principle of SR Flip Flop with its truth table. Also highlight the role of SR Flip Flop in switch debouncer circuit. **(08 Marks)**

b. With neat schematic diagram of master slave JK-FF, discuss its operation. Mention the advantages of JK-FF over master-slave SR-flip-flop. **(12 Marks)**

6 a. Design a 4-bit universal shift register using positive edge triggered D flip-flops to operate as shown in the table below Q6 (a) (12 Marks)

Select line S_0	Select line S_1	Data line selected	Register operation
0	0	I_0	HOLD
0	1	I_1	Shift RIGHT
1	0	I_2	Shift LEFT
1	1	I_3	Parallel load

Table Q6 (a)

b. Explain the working principle of a mod-8 binary ripple counter, configured using positive edge triggered T-FF. Also draw the timing diagram. (08 Marks)

7 a. Distinguish between Moore and Mealy model with necessary block diagrams. (08 Marks)

b. Give output function, excitation table and state transition diagram by analyzing the sequential circuit shown in figure Q7 (b) (12 Marks)

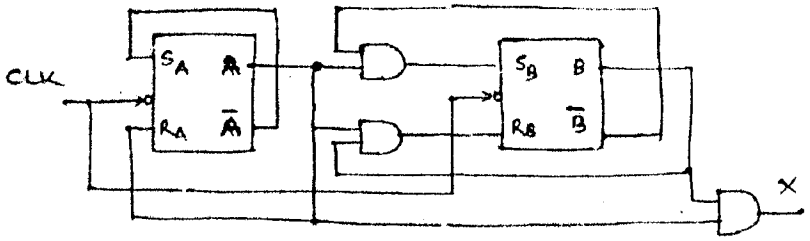

Fig. Q7 (b)

8 a. Construct Moore and Mealy state diagram that will detect input sequence 10110, when input pattern is detected, z is asserted high. Give state diagrams for each state. (10 Marks)

b. Design a cyclic mod 6 synchronous binary counter using JK flip-flop. Give the state diagram, transition table and excitation table. (10 Marks)

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06ES33

Third Semester B.E. Degree Examination, June-July 2009
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Express the P. O. S. equations in a Maxterms list (decimal notations) form. **(04 Marks)**

i) $F = f(a, b, c) = (a + \overline{b} + c)(a + \overline{b} + c)(\overline{a} + \overline{b} + c)$

ii) $F = f(A, B, C, D) = (A+\overline{B}+C+D)(A+\overline{B}+C+\overline{D})(\overline{A}+B+C+D)(\overline{A}+\overline{B}+C+D)(\overline{A}+B+\overline{C}+D)(\overline{A}+\overline{B}+\overline{C}+D)$

b. Reduce the following function using K-map technique and implement using gates. **(10 Marks)**

i) $f(P, Q, R, S) = \Sigma m\ (0, 1, 4, 8, 9, 10) + d(2, 11)$

ii) $f(A, B, C, D) = \pi M\ (0, 2, 4, 10, 11, 14, 15)$

c. Design a logic circuit with inputs P, Q, R so that output S is high whenever P is zero or whenever Q = R = 1. **(06 Marks)**

2 a. Using Quine Mccluskey Method and simply the following function.

$f(a, b, c, d) = \Sigma m\ (0, 1, 2, 3, 8, 9)$ **(10 Marks)**

b. Write the Map entered variable K-map for the Boolean function.

$f(w, x, y, z) = \Sigma m\ (2, 9, 10, 11, 13, 14, 15)$ **(10 Marks)**

3 a. Implement following multiple output function using 74LS138 and extend gates.

$F_1(A, B, C) = \Sigma m\ (1, 4, 5, 7)$

$F_2(A, B, C) = \pi M\ (2, 3, 6, 7)$ **(06 Marks)**

b. Implement full subtractor using decoder and write a truth table. **(08 Marks)**

c. Write a note on encoders. **(06 Marks)**

4 a. Design 2-bit comparator using gates. **(12 Marks)**

b. Implement the following Boolean function using 8 : 1 multiplexer.

$F(A, B, C, D) = \overline{A}B\overline{D} + ACD + \overline{B}CD + \overline{A}\overline{C}D$ **(08 Marks)**

PART – B

5 a. Clearly distinguish between

i) Synchronous and asynchronous circuits.

ii) Combinational and sequential circuits **(06 Marks)**

b. Explain the operation of clocked SR flip-flop. **(08 Marks)**

c. What is race around condition? Discuss in detail. **(06 Marks)**

6 a. Draw the logic diagrams for (i) SR latch (ii) Master – slave JK flip-flop (iii) Master-slave SR flip-flop. **(06 Marks)**

b. Explain the working of 4-bit asynchronous counter. **(06 Marks)**

c. Explain Johnson counter with its circuit diagram and timing diagram. **(08 Marks)**

7 a. Explain with suitable logic and timing diagram.

i) Serial-in serial-out shift register.

ii) Parallel-in parallel-out shift register. **(10 Marks)**

b. Explain the Meoly model and Moore model for clocked synchronous sequential network. **(10 Marks)**

8 a. Compare Moore and Meelay models. **(04 Marks)**

b. Design a synchronous counter using JK flip-flops to count in the sequence 0,1,2,4,5,6,0,1,2..... Use state diagram and state table. **(12 Marks)**

c. State the rules for state assignments. **(04 Marks)**

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06ES33

Third Semester B.E. Degree Examination, Dec.09/Jan.10
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Show that y = f (ABCD) = $\sum$ (0, 2, 5, 7, 8, 10, 13,15) is the complement of y = f(ABCD) = π(1, 3, 4, 6, 9, 11, 12, 14). Illustrate your answer using Karnaugh map to show the complement nature of the two equations. Realize both the functions using 7486 IC chip [Exclusive OR gates] only. **(12 Marks)**

b. Design a logic circuit that controls the passage of a signal 'A' according to the following requirement.
i) Output 'X' will equal 'A' when control inputs B and C are the same.
ii) 'X' will remain 'HIGH' when B and C are different
Implement the circuit using suitable gates. **(08 Marks)**

2 a. Simplify the following expression using Quine- McClusky technique. Implement the simplified circuit using basic gates: f (ABCD) = $\sum$ (1, 3, 4, 5, 6, 9, 11, 12, 13, 14). **(12 Marks)**

b. Simplify the following Boolean expression using VEM technique. [3 variable map].
f (ABCD) = $\sum$m (0, 4, 5, 6, 13, 14, 15) + dc (2, 7, 8, 9)

A	B	C	D	f
0	0	0	0	1
0	0	0	1	0
0	0	1	0	ϕ
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	ϕ

A	B	C	D	f
1	0	0	0	ϕ
1	0	0	1	ϕ
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

ϕ = don't care term. **(08 Marks)**

3 a. Design a logic circuit using a 3 to 8 logic decoder that has active low data inputs, an active HIGH enable and active low data outputs. Use such a decoder to realize the full adder circuit. **(08 Marks)**

b. Design a suitable BCD adder circuit using 74LS83 and a provision has to be made for self correction in case if the sum is not a valid BCD number format. **(12 Marks)**

4 a. Implement the following Boolean function using 4 :1 MUX
y (ABCD) = $\sum$m (0, 1, 2, 4, 6, 9, 12, 14). **(10 Marks)**

b. Design a circuit that accepts 2 unsigned 4 bit numbers and provides 3 outputs. The inputs are A_3 A_2 A_1 A_0 and B_3 B_2 B_1 B_0. Outputs are A = B, A > B and A < B. Draw the logic diagram. **(10 Marks)**

PART – B

5 a. Explain the following:
   i) Switch debouncing and it's elimination
   ii) Race around problem and its elimination. **(14 Marks)**

   b. Obtain the characteristic equation for the following flip flops:
   i) JK flip flop
   ii) SR flip flop. **(06 Marks)**

6 a. With the help of a diagram, explain the following with respect to shift register:
   i) Parallel in and serial out
   ii) Ring counter and twisted ring counter. **(08 Marks)**

   b. Design a Mod – 5 synchronous counter using JK flip flop. **(12 Marks)**

7 a. With a suitable example, explain Mealy and Moore model in a sequential circuit analysis. **(10 Marks)**

   b. A sequential circuit has one input and one output. The state diagram is as shown in Fig.7(b). Design a sequential circuit with 'T' flip flop. **(10 Marks)**

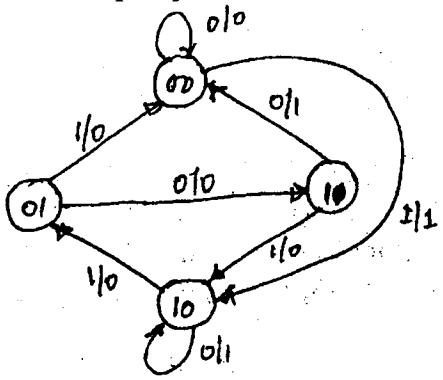

Fig.7(b).

8 a. Analyse the following sequential circuit shown in Fig.8(a) and obtain:
   i) Flip flop input and output equations.
   ii) Transition equation
   iii) Transition table
   iv) State table
   v) Draw the state diagram. **(12 Marks)**

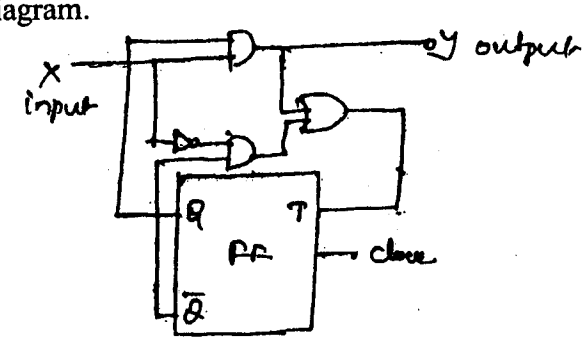

Fig.8(a).

   b. With a suitable example and appropriate state diagram, explain how to recognize a particular sequence. Ex: 1011. (Any sequence can be assumed). **(08 Marks)**

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06ES33

Third Semester B.E. Degree Examination, May/June 2010
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Simplify the following expressions using k – map. Implement the simplified expression using basic gates :
   i) $T = f(wxyz) = \sum m(2, 3, 4, 5, 13, 15) + \sum d(8, 9, 10, 11)$
   ii) $R = f(abcd) = \pi M(2, 3, 4, 6, 7, 10, 11, 12)$. **(12 Marks)**

b. Place the following equations into proper canonical form :
   i) $P = f(a, b, c) = ab' + ab' + bc$
   ii) $T = f(a, b, c)\ (a + b')\ (b' + c)$. **(04 Marks)**

c. Define the following terms :
   i) Minimum iii) Canonical sum of products
   ii) Maximum iv) Canonical product of sum. **(04 Marks)**

2 a. Simplify the logic function given below using variable entered mapping (VEM) technique :
   $f(a, b, c, d) = \sum m(2, 9, 10, 11, 13, 14, 15)$. **(08 Marks)**

b. Simplify the following function using Quine-McClusky minimization technique :
   $T = f(a, b, c, d) = \sum m(0, 1, 2, 3, 6, 7, 8, 9, 14, 15)$. **(12 Marks)**

3 a. Design a combinational logic circuit to output the 2's compliment of a 4-bit binary numbers:
   i) Construct the truth table
   ii) Simplify each output function using k-map and write reduced equations
   iii) Draw the resulting logic diagram. **(12 Marks)**

b. Construct a scheme to obtain a 4-to-16 line decoder using 74138 (3-8 line decoder). **(05 Marks)**

c. Write a note on encodes. **(03 Marks)**

4 a. Realize the following Boolean function $f(ABC) = \sum(0, 1, 3, 5, 7)$ using,
   i) 8 : 1mux(74151)
   ii) 4 : 1mux(74153). **(06 Marks)**

b. Design a comparator to check if two n-bit numbers are equal. Configure this using cascaded stage of 1 bit equality comparator. **(08 Marks)**

c. Implement full subtractor using gates and write a truth table. **(06 Marks)**

PART – B

5 a. Explain the operation of SR latch. Explain one of its applications. **(12 Marks)**

b. Draw the logic diagrams for
   i) Gated SR latch iii) Master slave JK flip flop
   ii) Master slave SR flip flop iv) Positive edge triggered 'D' flip flop. **(08 Marks)**

6 a. Differentiate between combinational logic circuit and sequential logic circuits. **(03 Marks)**

b. Explain universal shift register with the help of logic diagram, mode control table and symbol. **(09 Marks)**

c. Explain Jonson counter, with its circuit diagram, and timing diagram. **(08 Marks)**

7 a. Explain Moore and Meclay models for clocked synchronous sequential circuits. (10 Marks)

b. Construct the excitation table, transition table, state table and state diagram, for the Moore sequential circuit shown in Fig. Q7(b). (10 Marks)

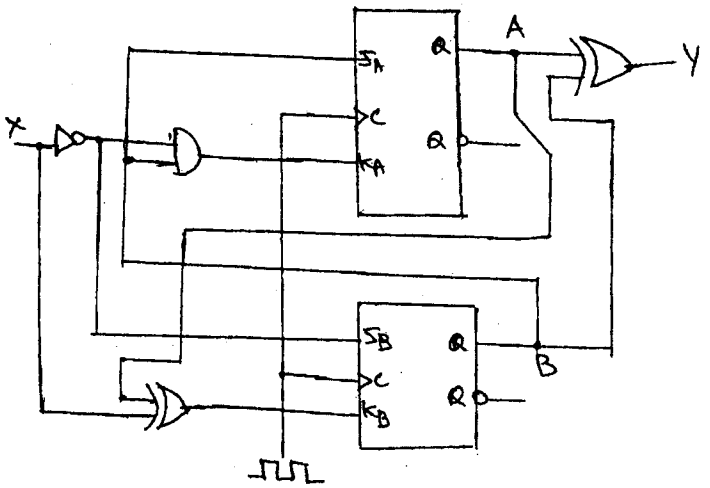

Fig. Q7(b)

8 a. Write a note on construction of state diagram. (05 Marks)

b. Design a counter using JK-flip flops whose counting sequence is 000, 001, 100, 110, 111, 101, 000 etc., by obtaining its minimal sum equations. (10 Marks)

c. Write a note on characteristic equations. (05 Marks)

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